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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/828,481	04/06/2001	Anthony William Jorgenson	KES-00-002	6775

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EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	8

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/828,481	Applicant(s) JORGENSON, ANTHONY WILLIAM	
	Examiner Clifford H Knoll	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to communication filed 4/8/04. Currently claims 1-35 are pending.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

Claim 34 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The serial control bus is unclear because its composition as a plurality of cards transmitting data on a data bus, and a controller coupled to the data bus is inconsistent with the meaning of a control bus. This might be amended to a "control bus *architecture*", but even then the control bus itself is not positively recited.

Claim Rejections - 35 USC § 102

Claims 1-31 and 33 stand rejected under 35 U.S.C. 102(e) as being anticipated by Shideler (US 6625163).

Regarding claims 1 and 16, Shideler discloses a controller and its method, and a plurality of connections with each first end coupled to a controller (e.g., col.8, lines 37-42) and a plurality of peripheral cards coupled to a second end (e.g., col.8, lines 37-42).

Regarding claims 2 and 17, Shideler also discloses peripheral cards including transmit and collision connection and each are connected to a separate second end of said respective dedicated one of said plurality of connections (e.g., col.7, lines 39-45).

Regarding claims 3 and 18, Shideler also discloses a transmit lead and collision lead, each said lead separately coupled to said second end of said respective dedicated one of said plurality of connections (e.g., col.7, lines 39-45).

Regarding claims 4 and 19, Shideler also discloses a logic device (e.g., col.7, line 16).

Regarding claims 6 and 21, Shideler further discloses the logic device having a plurality of drivers each dedicated to receive signals from a particular peripheral card (e.g., col.7, lines 8-11), the controller is configured to individually disable one or more of said plurality of drivers (e.g., col.1, lines 60-67, col.7, lines 43-45).

Regarding claims 7 and 22, Shideler further discloses a control unit and the method of generating a control signal (e.g., col.7, lines 8-9), a plurality of OR gates (e.g., col.7, line 9), and performing an AND operation to outputs of said OR gates and providing output to said controller (e.g., Figure 2, item 203).

Regarding claims 8 and 23, Shideler also discloses a hard wire connection (e.g., col.3, lines 23-26).

Regarding claims 9 and 24, Shideler also discloses one of a MPC 860, MPC 850, and MPC8260 processor (e.g., col.8, lines 43-49)

Regarding claims 11 and 26, Shideler also discloses separation by a distance ranging from one inch to seven feet (e.g., col. 3, lines 9-16).

Regarding claims 15 and 30, Shideler also discloses a bus that may be configured to support half duplex mode and full duplex mode communication (e.g., col.4, lines 30-39).

Regarding claim 31, Shideler discloses detecting a signal communication failure on a data bus (e.g., col.7, lines 53-54), performing a control bus integrity check and isolating the origin of said signal communication failure to a particular peripheral device (e.g., col.7, lines 26-27, col.13, lines 37-44).

Regarding claim 33, Shideler also discloses detecting a combined bus signal (e.g., col. 7, lines 9-10) and determining whether a transmit signal from a peripheral device is continuously low (col.7, line 7).

Claims 31-32 and 34-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Barenys (US 2002/0108076).

Regarding claim 31, Barenys discloses detecting a signal communication failure (e.g., para. 23), performing a control bus integrity check in response, and isolating the origin of the failure to a particular peripheral device (e.g., para. 36).

Regarding claim 32, Barenys also discloses the failure includes lack of response to a controller request or poll (e.g., para. 23)

Regarding claim 34, Barenys discloses the control bus with a plurality of peripheral cards to transmit data; and a controller, coupled to the data bus and separately coupled to each of the plurality of peripheral cards (e.g., para. 25, "switches 301-304").

Regarding claim 35, Barenys also discloses being configured to determine whether the fault occurred on one of the plurality of peripheral cards or on the controller (e.g., Figure 3, "Switch 301" and "Switch 303").

Claims 31-32 and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Burri (US 5193177).

Regarding claim 31, Burri discloses detecting a signal communication failure (e.g., col. 2, lines 40-45), performing a control bus integrity check in response, and isolating the origin of the failure to a particular peripheral device (e.g., col. 2, lines 59-61).

Regarding claim 32, Burri also discloses the failure includes lack of response to a controller request or poll (e.g., col. 2, lines 54-58).

Regarding claim 34, Burri discloses the control bus with a plurality of peripheral cards to transmit data; and a controller, coupled to the data bus and separately coupled to each of the plurality of peripheral cards (e.g., col. 2, lines 37-40).

Claim Rejections - 35 USC § 103

Claims 5 and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Shideler in view of Webber (US 6381213).

Regarding claims 5 and 20, Shideler discloses a logic device. Shideler does not expressly disclose a particular implementation of the logic device as being an FPGA;

however, this is a widely known means of implementing a logic device, as exemplified by Webber.

Webber discloses implementing logic for a communications interface using an FPGA (col.11, lines 26-29). It would be obvious to combine Webber with Shideler because the Webber teaches the common implementation detail of using an FPGA to implement a logic device for a bus controller, such as that of Shideler. Therefore it would be obvious to one of ordinary skill in the art to combine Webber with Shideler at the time the invention was made.

Claims 10, 14, 25, and 29 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Shideler in view of AMD's benchmarking data sheet ("AM186 CC/CH microcontroller HDLC benchmarking data").

Regarding claims 10, 14, 25, and 29, Shideler also claims the use of various embodiments of HDLC protocol (e.g., col.2, lines 51-60). Shideler does not expressly mention the particular data rate that is recited; however, it is a manifestly common feature of practicing the HDLC protocol to operate at a broad range of data rates, as exemplified by AMD's benchmarking data sheet. AMD discloses a broad range of data rates, from the standard T1/E1 data rate (2.048 Mbps), through 3 Mbps to 7 Mbps, and beyond and teaches their application regarding tradeoffs in buffer size and computational load. It would be obvious to one of ordinary skill in the art to operate Shideler's invention at a frequency range between approximately 3 MHz to 6 MHz, or at 6 MHz at the time the invention was made.

Claims 12-13, 27-28 rejected under 35 U.S.C. 103(a) as being unpatentable over Shideler in view of Brolin (US 6359859).

Shideler specifically mentions a wide variety of communications networks, but he does not explicitly express the particular embodiment of an optical data communications network. However, this is quite standard in communications network controllers as exemplified by Brolin.

Regarding claims 12 and 27, Shideler discloses the use of his invention in a "wide variety of standard WANs, LANs, and proprietary networks" with "many physical interface options" (e.g., col.3, lines 10-17). Brolin discloses an optical communications network each configured to receive and transmit electrical and optical signals (col.1, lines 16-21).

Regarding claims 13 and 28, Brolin also discloses one of OC-3, OC-12, and OC-48, and one of STS-3, STS-12, and STS-48 (col.1, lines 36-47).

It would be obvious to combine Brolin with Shideler because the OC-N and STS-N signal series are standard protocols in used with controllers, such as the controller of Shideler. Therefore it would be obvious to one of ordinary skill in the art to combine Brolin with Shideler at the time the invention was made.

Response to Arguments

Applicant's arguments filed 4/8/04 regarding the rejection using Shideler have been fully considered but they are not persuasive.

Regarding claims 1 and 16, Applicant argues that distinct from the claimed "dedicated connections, "Shideler discloses a shared connection between a controller module and application modules"; and that "[w]hereas claims 1 and 16 recite a plurality of connections coupled to the controller, Shideler only has a single link to the controller. Since there is no plurality of connections, it follows that Shideler does not disclose a plurality of peripheral cards individually coupled to the plurality of connections" (p. 12). However, while Shideler does indeed teach a sharing a connection, the dedicated connections as claimed are taught as well. Figure 1 shows that the controller comprises dedicated connections, one for standard HDLC communication, and one for OEM HDLC communication. Shideler notes: "subsequent discussion focuses on the HDLC A/B differential bus access control logic. The OEM HDLC bus access control logic operates in a similar fashion. In the preferred embodiment, both circuits are included in one programmable logic device" (col. 3, lines 36-41).

Thus claims 1 and 16 stand rejected.

Regarding claims 2 and 17, Applicant argues that Shideler does note teach or suggest "a peripheral card with a dedicated transmit connection and separate collision connection" (p. 13); however, Shideler does in fact disclose a transmit connection and separate collision connection (e.g., Figure 4, "hdlc_ab_tx" and "hdlc_a_rx", respectively).

Thus claims 2 and 17 stand rejected.

Applicant's arguments with respect to claim 31 rejection using Wight have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mori (US 6678839) discloses a different control bus architecture for isolating faults. Follett (US 4872163) discloses an alternate control bus architecture, which includes a collision connection.

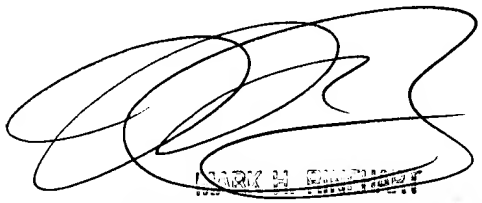
THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 703-305-8656. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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